WHAT IS CLAIMED IS:

1. A method of programming a non-volatile memory device including a string of serially connected memory cell transistors with each memory cell transistor of the string being connected to a different word line, the method comprising:

applying a pass voltage to a first word line connected to a first memory cell transistor of the string;

applying a coupling voltage to a second word line connected to a second memory cell transistor of the string wherein the coupling voltage is greater than a ground voltage of the memory device and wherein the pass voltage and the coupling voltage are different; and

while applying the pass voltage to the first word line and while applying the coupling voltage to the second word line, applying a program voltage to a third word line connected to a third memory cell transistor of the string, the third memory cell transistor being programmed responsive to applying the program voltage to the third word line wherein the second memory cell transistor is between the first and third memory cell transistors of the serially connected string.

2. A method according to Claim 1 further comprising:

applying the pass voltage to a fourth word line connected to a fourth memory cell transistor of the string wherein the first memory cell transistor is serially connected between the fourth memory cell transistor and the second memory cell transistor.

3. A method according to Claim 1 wherein the coupling voltage is greater than the pass voltage.

4. A method according to Claim 1 wherein each memory cell transistor of the string stores one bit of data.

5. A method according to Claim 1 wherein each memory cell of the transistor of the string stores a plurality of bits of data.

6. A method according to Claim 1 further comprising:

applying a decoupling voltage to a fourth word line connected to a fourth memory cell transistor of the string wherein the fourth memory cell transistor of the string is serially connected between the first and second memory cell transistors;

wherein the decoupling voltage is less than the pass voltage, less than the coupling voltage, and less than the program voltage; and

wherein the program voltage is applied to the third word line while applying the pass voltage to the first word line, while applying the coupling voltage to the second word line, and while applying the decoupling voltage to the fourth word line.

7. A method according to Claim 6 wherein the decoupling voltage comprises a ground voltage of the memory device.

8. A method according to Claim 6 wherein the decoupling voltage is less than a ground voltage of the memory device.

9. A method according to Claim 6 further comprising:

before applying the decoupling voltage to the fourth word line, applying a preliminary voltage to the fourth word line wherein the preliminary voltage is greater than the decoupling voltage and wherein the decoupling voltage is applied to the fourth word line before applying the program voltage to the third word line.

10. A method according to Claim 9 wherein the preliminary voltage is equal to the pass voltage.

11. A method according to Claim 1 wherein the non-volatile memory device includes a second string of serially connected memory cell transistors with a memory cell transistor of the second string being connected to the third word line, the method further comprising:

before applying the program voltage, precharging a channel of the third memory cell transistor with a first precharge voltage; and

before applying the program voltage, precharging a channel of the memory cell transistor of the second string connected to the third word line with a second voltage different than the first voltage.

12. A method according to Claim 11 wherein the first voltage is a ground voltage of the memory device and wherein the second voltage is a difference between a power supply voltage of the memory device and a threshold voltage of the select transistor of the second string.

13. A method of programming a non-volatile memory device including string of serially connected memory cell transistors with each memory cell transistor of the string being connected to a different word line, the method comprising:

applying a decoupling voltage to a first word line connected to a first memory cell transistor of the string;

applying a coupling voltage to a second word line connected to a second memory cell transistor of the string wherein the coupling voltage is greater than the decoupling voltage; and

while applying the decoupling voltage to the first word line and while applying the coupling voltage to the second word line, applying a program voltage to a third word line connected to a third memory cell transistor of the string, the third memory cell transistor being programmed responsive to applying the program voltage to the third word line wherein the second memory cell transistor is between the first and third memory cell transistors of the serially connected string.

14. A method according to Claim 13 further comprising:

before applying the decoupling voltage to the first word line, applying a preliminary voltage to the first word line wherein the preliminary voltage is greater that the decoupling voltage and wherein the decoupling voltage is applied to the first word line before applying the program voltage to the third word line.

15. A method according to Claim 14 further comprising:

applying a pass voltage to a fourth word line connected to a fourth memory cell transistor of the string wherein the first memory cell transistor is serially connected between the fourth and second memory cell transistors, wherein the pass voltage is greater than the decoupling voltage, and wherein the pass voltage is equal to the preliminary voltage.

16. A method according to Claim 13 further comprising:

applying a pass voltage to a fourth word line connected to a fourth memory cell transistor of the string wherein the first memory cell transistor is serially connected between the fourth and second memory cell transistors, wherein the pass voltage is greater than the decoupling voltage.

17. A method according to Claim 16 further comprising:

applying the pass voltage to a fifth word line connected to a fifth memory

cell transistor of the string wherein the fourth memory cell transistor is serially connected between the fifth and first memory cell transistors.

18. A method according to Claim 16 wherein the coupling voltage is greater than or equal to the pass voltage.

19. A method according to Claim 16 wherein the coupling voltage is greater than the pass voltage.

20. A method according to Claim 13 wherein each memory cell of the string stores one bit of data.

21. A method according to Claim 13 wherein each memory cell of the string stores a plurality of bits of data.

22. A method according to Claim 13 wherein the decoupling voltage comprises a ground voltage of the memory device.

23. A method according to Claim 13 wherein the decoupling voltage is less than a ground voltage of the memory device.

24. A method according to Claim 13 wherein the non-volatile memory device includes a second string of serially connected memory cell transistors with a memory cell transistor of the second string being connected to the third word line, the method further comprising:

before applying the program voltage, precharging a channel of the third memory cell transistor with a first precharge voltage; and

before applying the program voltage, precharging a channel of the memory cell transistor of the second string connected to the third word line with a second voltage different than the first voltage.

25. A method according to Claim 24 wherein the first voltage is a ground voltage of the memory device and wherein the second voltage is a difference between a power supply voltage of the memory device and a threshold voltage of the select transistor of the second string.

26. A non-volatile memory device comprising:

a string of serially connected memory cell transistors

a plurality of word lines with each word line being connected to a different one of the serially connected memory cell transistors; and

a row selection circuit connected to the plurality of word lines, the row selection circuit being configured to apply a pass voltage to a first word line connected to a first memory cell transistor of the string, the row selection circuit being configured to apply a coupling voltage to a second word line connected to a second memory cell transistor of the string wherein the coupling voltage is greater than a ground voltage of the memory device and wherein the pass voltage and the coupling voltage are different, and the row selection circuit being configured to apply a program voltage to a third word line connected to a third memory cell transistor of the string while applying the pass voltage to the first word line and while applying the coupling voltage to the second word line, the third memory cell transistor being programmed responsive to applying the program voltage to the third word line wherein the second memory cell transistor is between the first and third memory cell transistors of the serially connected string.

27. A non-volatile memory device according to Claim 26 wherein the row selection circuit is further configured to apply the pass voltage to a fourth word line connected to a fourth memory cell transistor of the string wherein the first memory cell transistor is serially connected between the fourth memory cell transistor and the second memory cell transistor.

28. A non-volatile memory device according to Claim 26 wherein the coupling voltage is greater than the pass voltage.

29. A non-volatile memory device according to Claim 26 wherein each memory cell transistor of the string stores one bit of data.

30. A non-volatile memory device according to Claim 26 wherein each memory cell of the transistor of the string stores a plurality of bits of data.

31. A non-volatile memory device according to Claim 26 wherein the row selection circuit is further configured to apply a decoupling voltage to a fourth word line connected to a fourth memory cell transistor of the string wherein the fourth

memory cell transistor of the string is serially connected between the first and second memory cell transistors, wherein the decoupling voltage is less than the pass voltage, less than the coupling voltage, and less than the program voltage, and wherein the program voltage is applied to the third word line while applying the pass voltage to the first word line, while applying the coupling voltage to the second word line, and while applying the decoupling voltage to the fourth word line.

32. A non-volatile memory device according to Claim 31 wherein the decoupling voltage comprises a ground voltage of the memory device.

33. A non-volatile memory device according to Claim 31 wherein the decoupling voltage is less than a ground voltage of the memory device.

34. A non-volatile memory device according to Claim 31 wherein the row selection circuit is further configured to apply a preliminary voltage to the fourth word line before applying the decoupling voltage to the fourth word line, wherein the preliminary voltage is greater than the decoupling voltage and wherein the decoupling voltage is applied to the fourth word line before applying the program voltage to the third word line.

35. A non-volatile memory device according to Claim 34 wherein the preliminary voltage is equal to the pass voltage.

36. A non-volatile memory device according to Claim 26 further comprising:

a second string of serially connected memory cell transistors with a memory cell transistor of the second string being connected to the third word line; and

a precharge circuit coupled to the first and second strings of serially connected memory cell transistors wherein the precharge circuit is configured to precharge a channel of the third memory cell transistor with a first precharge voltage before applying the program voltage, and wherein the precharge circuit is configured to precharge a channel of the memory cell transistor of the second string connected to the third word line with a second voltage different than the first voltage before applying the program voltage.

37. A non-volatile memory device according to Claim 36 wherein the first

voltage is a ground voltage of the memory device and wherein the second voltage is a difference between a power supply voltage of the memory device and a threshold voltage of a select transistor of the second string.

38. A non-volatile memory device comprising:

a string of serially connected memory cell transistors;

a plurality of word lines with each word line being connected to a different one of the serially connected memory cell transistors; and

a row selection circuit connected to the plurality of word lines, the row selection circuit being configured to apply a decoupling voltage to a first word line connected to a first memory cell transistor of the string, the row selection circuit being configured to apply a coupling voltage to a second word line connected to a second memory cell transistor of the string wherein the coupling voltage is greater than the decoupling voltage, and the row selection circuit being configured to apply a program voltage to a third word line connected to a third memory cell transistor of the string while applying the decoupling voltage to the first word line and while applying the coupling voltage to the second word line, the third memory cell transistor being programmed responsive to applying the program voltage to the third word line wherein the second memory cell transistor is between the first and third memory cell transistors of the serially connected string.

39. A non-volatile memory device according to Claim 38 wherein the row selection circuit is further configured to apply a preliminary voltage to the first word line before applying the decoupling voltage to the first word line, wherein the preliminary voltage is greater that the decoupling voltage and wherein the decoupling voltage is applied to the first word line before applying the program voltage to the third word line.

40. A non-volatile memory device according to Claim 39 wherein the row selection circuit is further configured to apply a pass voltage to a fourth word line connected to a fourth memory cell transistor of the string wherein the first memory cell transistor is serially connected between the fourth and second memory cell transistors, wherein the pass voltage is greater than the decoupling voltage, and wherein the pass voltage is equal to the preliminary voltage.

41. A non-volatile memory device according to Claim 38 wherein the row

selection circuit is further configured to apply a pass voltage to a fourth word line connected to a fourth memory cell transistor of the string wherein the first memory cell transistor is serially connected between the fourth and second memory cell transistors, wherein the pass voltage is greater than the decoupling voltage.

42. A non-volatile memory device according to Claim 41 wherein the row selection circuit is further configured to apply the pass voltage to a fifth word line connected to a fifth memory cell transistor of the string wherein the fourth memory cell transistor is serially connected between the fifth and first memory cell transistors.

43. A non-volatile memory device according to Claim 41 wherein the coupling voltage is greater than or equal to the pass voltage.

44. A non-volatile memory device according to Claim 41 wherein the coupling voltage is greater than the pass voltage.

45. A non-volatile memory device according to Claim 38 wherein each memory cell of the string stores one bit of data.

46. A non-volatile memory device according to Claim 38 wherein each memory cell of the string stores a plurality of bits of data.

47. A non-volatile memory device according to Claim 38 wherein the decoupling voltage comprises a ground voltage of the memory device.

48. A non-volatile memory device according to Claim 38 wherein the decoupling voltage is less than a ground voltage of the memory device.

49. A non-volatile memory device according to Claim 38 further comprising:

a second string of serially connected memory cell transistors with a memory cell transistor of the second string being connected to the third word line;

a precharge circuit connected to the first and second strings of serially connected memory cells, the precharge circuit being configured to precharge a channel of the third memory cell transistor with a first precharge voltage before applying the program voltage, and the precharge circuit being configured to precharge

a channel of the memory cell transistor of the second string connected to the third word line with a second voltage different than the first voltage before applying the program voltage.

50. A non-volatile memory device according to Claim 49 wherein the first voltage is a ground voltage of the memory device and wherein the second voltage is a difference between a power supply voltage of the memory device and a threshold voltage of a select transistor of the second string.

51. A program method of a non-volatile semiconductor memory device which includes strings each connected to corresponding bit lines and each having a plurality of memory cell transistors, the memory cell transistors being connected in series between first and second select transistors and to corresponding word lines, the program method comprising the steps of:

supplying a coupling voltage to at least one first word line and a decoupling voltage to a second word line; and

supplying a program voltage to a third word line connected to a memory cell transistor to be programmed, wherein the first word line is closely adjacent to the third word line and the second word line is closely adjacent word line to the first word line; and wherein the coupling voltage is higher than the decoupling voltage.

52. The program method according to claim 51, wherein a pass voltage is supplied to remaining word lines.

53. The program method according to claim 52, wherein the coupling voltage is equal to or higher than the pass voltage.

54. The program method according to claim 53, further comprising the step of precharging a channel of the memory cell transistor to be programmed with a first voltage and a channel of a memory cell transistor to be program-inhibited with a second voltage.

55. The program method according to claim 54, wherein the first voltage is a ground voltage and the second voltage is (Vcc-Vth), the Vth being a threshold voltage of the first select transistor and the Vcc being a power supply voltage.

56. The program method according to claim 51, wherein each of the memory cell transistors stores 1-bit data.

57. The program method according to claim 51, wherein each of the memory cell transistors stores multi-bit data.

58. The program method according to claim 51, wherein the decoupling voltage is a ground voltage.

59. The program method according to claim 51, wherein the decoupling voltage is lower than a ground voltage.

60. A program method of a non-volatile semiconductor memory device which includes strings each connected to corresponding bit lines and each having a plurality of memory cell transistors, the memory cell transistors being connected in series between first and second select transistors and to corresponding word lines, the program method comprising the steps of:

charging a channel of a memory cell transistor to be programmed with a first voltage and a channel of a memory cell transistor to be program-inhibited with a second voltage, respectively;

supplying a coupling voltage to first two word lines, a decoupling voltage to second two word lines, and a pass voltage to remaining word lines, the first word lines being closely adjacent to a third word line connected to the memory cell transistor to be programmed and the second word lines being closely adjacent to the first word line, respectively; and

supplying a program voltage to the third word line, wherein the decoupling voltage is lower than the coupling and pass voltages; and wherein the coupling voltage is equal to or lower than the pass voltage.

61. The program method according to claim 60, wherein the first voltage is a ground voltage and the second voltage is (Vcc-Vth), the Vth being a threshold voltage of the first select transistor and the Vcc being a power supply voltage.

62. The program method according to claim 60, wherein each of the

memory cell transistors stores 1-bit data.

63. The program method according to claim 60, wherein each of the memory cell transistors stores multi-bit data.

64. The program method according to claim 60, wherein the decoupling voltage is a ground voltage.

65. The program method according to claim 60, wherein the decoupling voltage is lower than a ground voltage.

66. A program method of a non-volatile semiconductor memory device which includes strings each connected to corresponding bit lines and each having a plurality of memory cell transistors, the memory cell transistors being connected in series between first and second select transistors and to corresponding word lines, the program method comprising the steps of:

charging a channel of a memory cell transistor to be programmed with a first voltage and a channel of a memory cell transistor to be program-inhibited with a second voltage, respectively;

supplying a coupling voltage to a first word line and a pass voltage to remaining word lines, the first word line being closely adjacent to a third word line connected to the memory cell transistor to be programmed; and

supplying a program voltage to the third word line, wherein the coupling voltage is equal to or higher than the pass voltage.

67. The program method according to claim 66, wherein the first voltage is a ground voltage and the second voltage is (Vcc-Vth), the Vth being a threshold voltage of the first select transistor and the Vcc being a power supply voltage.

68. The program method according to claim 66, wherein each of the memory cell transistors stores 1-bit data.

69. The program method according to claim 66, wherein each of the memory cell transistors stores multi-bit data.

70. A non-volatile semiconductor memory device comprising:

a plurality of bit lines;

a plurality of word lines;

a plurality of cell strings connected to the bit lines, respectively, each of the cell strings being connected between a corresponding bit line and a common source line and having a first select transistor connected to a string select line, a second select transistor connected to a ground select line, and a plurality of memory cell transistors connected in series between the first and second transistors and to corresponding word lines respectively;

a row selector circuit connected to the string select line, the word lines and the ground select line, for selecting a first one of the word lines; and

a precharge circuit for supplying a first voltage to channels of memory cell transistors to be programmed and a second voltage to channels of memory cell transistors to be program-inhibited among memory cell transistors at a program operation, the transistors to be programmed and program-inhibited being connected to the first word line,

wherein before a program voltage is supplied to the first word line, the row selector circuit supplies a coupling voltage to a second word line closely adjacent to the first word line, a decoupling voltage to a third word line closely adjacent to the second word line, and a pass voltage to remaining word lines, the coupling voltage being higher than the decoupling voltage.

71. The memory device according to claim 70, wherein the first voltage is a ground voltage and the second voltage is (Vcc-Vth), the Vth being a threshold voltage of the first select transistor and the Vcc being a power supply voltage.

72. The memory device according to claim 70, wherein each of the memory cell transistors stores 1-bit data.

73. The memory device according to claim 70, wherein each of the memory cell transistors stores multi-bit data.

74. The memory device according to claim 70, wherein the decoupling voltage is a ground voltage.

75. The memory device according to claim 70, wherein the decoupling

voltage is lower than a ground voltage.

76. The memory device according to claim 70, wherein the coupling voltage is equal to or higher than the pass voltage.

77. The memory device according to claim 70, wherein the coupling voltage is lower than the pass voltage.

78. A non-volatile semiconductor memory device comprising:

a plurality of bit lines;

a plurality of word lines;

a plurality of cell strings connected to the bit lines, respectively, each of the cell strings being connected between a corresponding bit line and a common source line and having a first select transistor connected to a string select line, a second select transistor connected to a ground select line, and a plurality of memory cell transistors connected in series between the first and second transistors and to corresponding word lines respectively;

a row selector circuit connected to the string select line, the word lines and the ground select line, for selecting a first one of the word lines; and

a precharge circuit for supplying a first voltage to channels of memory cell transistors to be programmed and a second voltage to channels of memory cell transistors to be program-inhibited among memory cell transistors at a program operation, the transistors to be programmed and program-inhibited being connected to the first word line,

wherein before a program voltage is supplied to the first word line, the row selector circuit supplies a coupling voltage to a second word line closely adjacent to the first word line and a pass voltage to remaining word lines, the coupling voltage being equal to or higher than the pass voltage.

79. The memory device according to claim 78, wherein the first voltage is a ground voltage and the second voltage is (Vcc-Vth), the Vth being a threshold voltage of the first select transistor and the Vcc being a power supply voltage.

80. The memory device according to claim 78, wherein each of the memory cell transistors stores 1-bit data.